Session 14 Overview

Baseband Signal Processing

Chair: Steffen Paul, *Infineon Technologies, Neubiberg, Germany*

Associate Chair: Tzi-Dar Chiueh, *National Taiwan University, Taipei, Taiwan*

The computational demand of today's wireless standards has reached a level that requires a high degree of CMOS integration. In this session, different aspects of such implementations are discussed at the block, architectural, and system level. Clock recovery as an important module in a design is discussed. Decoding at high data rates expands the application of wireless communications. In the emerging market of multi-standard terminals, new architectural proposals are an active area of investigation. Among such proposals is Network-on-Chip as an interconnect technology between processing elements. Base station signal processing for WCDMA/HSPA demands high integration and high performance while on the terminal side, ultra low-cost platforms attract market share. MIMO as a transmission technology enables high data rates and more efficient use of spectrum.

Paper 14.1 from MediaTek presents the first RTL cell-based clock recovery circuit for optical disc drives. The clock recovery circuit can be easily migrated to other technologies because it is synthesizable.

In Paper 14.2, from Intel, an on-die special purpose channel decoding accelerator for high-performance processors is shown. It reaches a data rate of 1.9Gb/s and is reconfigurable.

Network-on-Chip (NoC) for communication among 20 processing nodes for use in telecommunications applications is presented in Paper 14.3 by CEA-LETI, France Telecom, Mitsubitshi, STMicroelectronics. This chip explores an architecture for future multi-mode wireless terminals.

Different goals of integration for cellular wireless chips are presented in the next three papers of this session. In Paper 14.4 from ETH, ACP, Miromico, a power and area-efficient baseband ASIC realization is described. The design contains a multi-mode front-end suited for EDGE, WCDMA, and WLAN modes. Furthermore, the baseband processing for WCDMA and HSDPA is added as hardware accelerators.

The integration of 3 DSP cores and support of WCDMA/HSPA+ base station signal processing on a single chip is reported in Paper 14.5 from TI. This allows for a reduction in the cost of base stations.

Paper 14.6 from Infineon describes the full integration of the power management unit into a GSM compliant baseband radio GSM chip, helping to accelerate the arrival of ultra low-cost terminals.

A PHY and MAC processor for draft 802.11n, featuring a 3x3 MIMO system, is presented in Paper 14.7 from Atheros Communications. The system transmits data at a maximum rate of 300Mb/s or at a maximum range of 700ft.

14.1 RTL-based Clock Recovery Architecture with All-Digital Duty-Cycle Correction **8:30 AM**

P-Y. Wang, MediaTek, Hsinchu, Taiwan

An RTL-based clock-recovery (CR) loop offers jitter filtering and frequency multiplication with a data-rate range from 76 to 496Mb/s. The design has direct digital phase shift capability with 20ps resolution for generating write-pulse recording sequences and digital duty-cycle correction for generating 50% duty-cycle clocks. The CR loop occupies 0.08mm^2 in 0.13µm CMOS and consumes 12mW with 1.2V supply at a channel rate of 496Mb/s.

14.2 A 1.9Gb/s 358mW 16-to-256 State Reconfigurable Viterbi Accelerator in 90nm CMOS **9:00 AM**

M. Anders, Intel, Hillsboro, OR

A 16-to-256 state coarse-grain reconfigurable Viterbi accelerator fabricated in 1.3V, 90nm dual-V_t CMOS technology is described for 3.8GHz operation, with 1.9Gb/s data rate in 32-state mode. Radix-4 ripple-carry ACS circuits, reconfigurable path metric read/write control and tree-bitline traceback memory circuits with programmable ring-buffer decoders enable 358mW total power, measured at 1.3V, 50°C, with performance scalable to 2.35Gb/s at 1.7V, 50°C.

14.3 A Telecom Baseband Circuit based on an Asynchronous Network-on-Chip **9:30 AM**

D. Lattard, CEA-LETI, Grenoble, France

The FAUST chip integrates a baseband processing architecture in which communications between IPs are supported by an asynchronous network-on-chip (NoC). This distributed and modular structure facilitates physical implementation and power management. A 20-node NoC is implemented in 79.5mm^2 using 0.13µm 6M CMOS to address 100Mb/s telecom systems.

14.4 A 50mW HSDPA Baseband Receiver ASIC with Multimode Digital Front-End **10:15 AM**

C. Martelli, ETH, Zurich, Switzerland

A multimode digital front-end for EDGE, WCDMA, and WLAN modes and a WCDMA/HSDPA receiver is implemented in 0.13µm 1P6M CMOS technology occupying 5.15mm^2 and dissipating 0.8/48/31mW in EDGE/HSDPA/WLAN modes, respectively.

14.5 A 65nm C64x+™ Multi-Core DSP Platform for Communications Infrastructure **10:45 AM**

S. Agarwala, Texas Instruments, Dallas, TX

The combined processing power of three 1+GHz DSP cores and 65nm 7M CMOS integration delivers a WCDMA macro base-station on a single chip. The 300M transistor IC can perform up to 24000MIPS, 8000 16b MMACs per second, coupled with symbol-rate and chip-rate acceleration and dissipates less than 6W.

14.6 A GSM Baseband Radio in 0.13µm CMOS with Fully Integrated Power-Management **11:15 AM**

M. Hammes, Infineon Technologies, Duisburg, Germany

A GSM-compliant baseband radio with integrated power-management unit (PMU) is fabricated in a 0.13µm CMOS process. Challenges due to additional integration of the PMU, including electrical and thermal cross-coupling and high-voltage requirements are addressed.

14.7 An Integrated Draft 802.11n Compliant MIMO Baseband and MAC Processor **11:45 AM**

P. Petrus, Atheros Communications, Santa Clara, CA

A 3×3 MIMO baseband and MAC processor in 0.18µm 6M CMOS occupies 62.1mm^2 and dissipates (Tx/Rx) 1379/1200mW at 1.8V including ADCs, DACs, and PCI/PCIe PHY. The integrated BB and MAC delivers up to 300Mb/s in 40MHz bandwidth, greater than 150Mb/s TCP throughput best case and a maximum range of 700ft range.